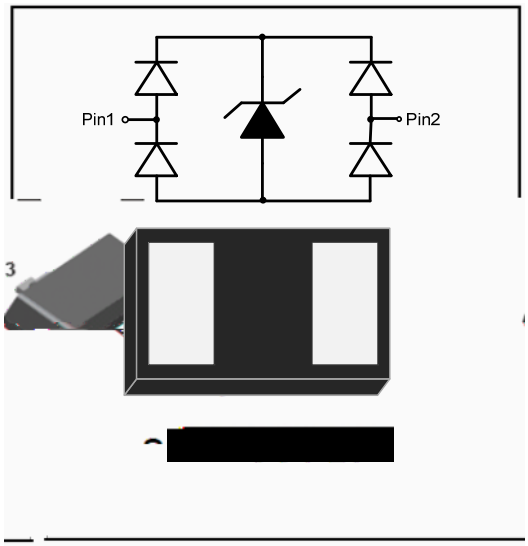
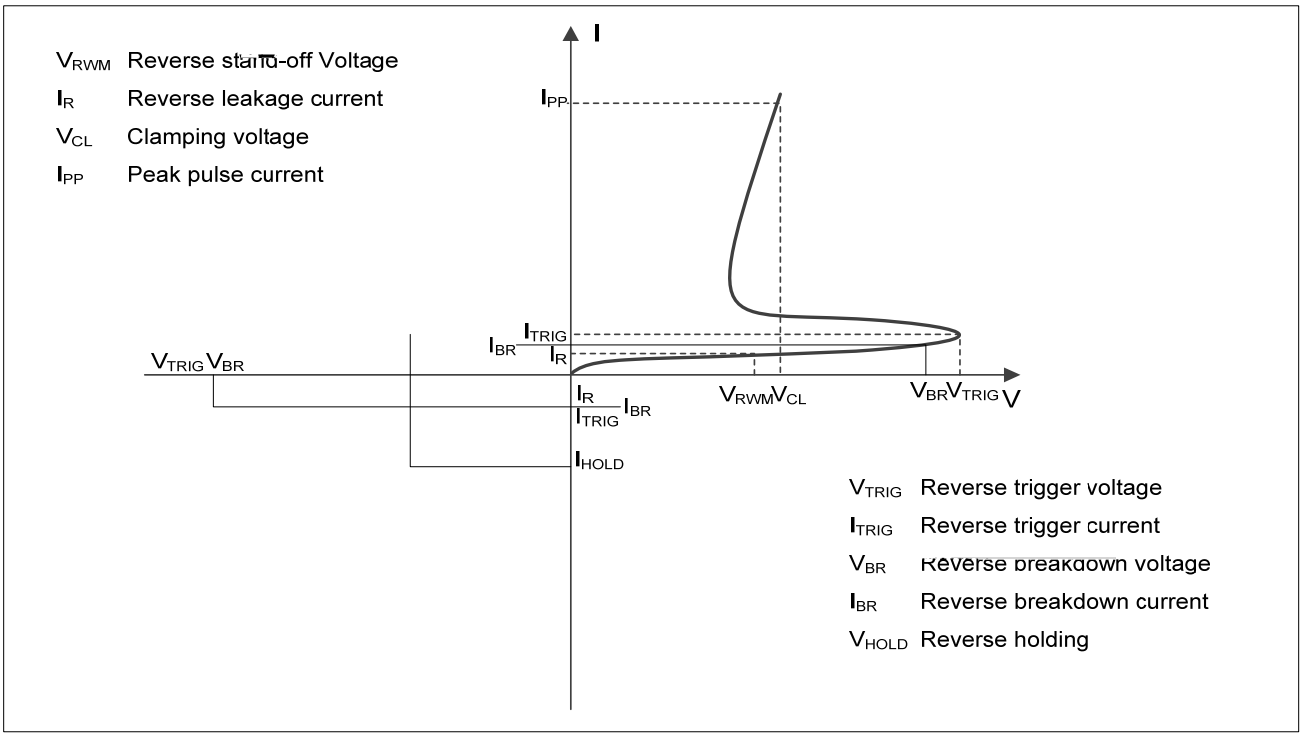


” Stand-off voltage: 18V Max
” Transient protection for each line according to IEC61000-4-2(ESD): ±15kV (contact)
IEC61000-4-5(surge): 4A (8/20 s)
” Ultra-low capacitance: C_J = 0.35pF typ
” Ultra-low leakage current: I_R < 1nA typ.
” Low clamping voltage: V_{CL} =10V typ. @ I_{PP} = 16A (TLP)
” Solid-state silicon technology

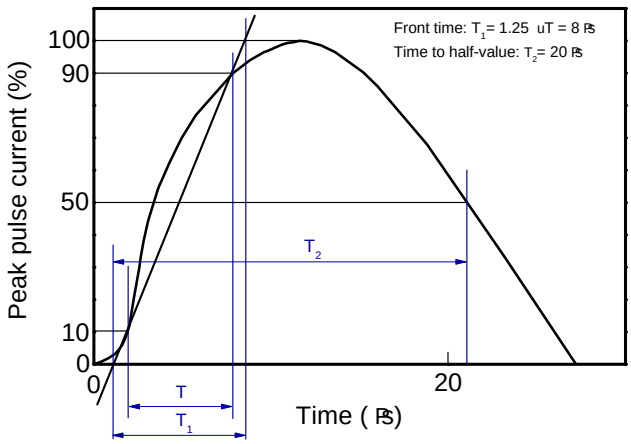
” : DFN1002L
” : Tin plated leads, solderable per J-STD-002 and JESD22-B102
” Cathode line denotes the cathode end
” 8U

V



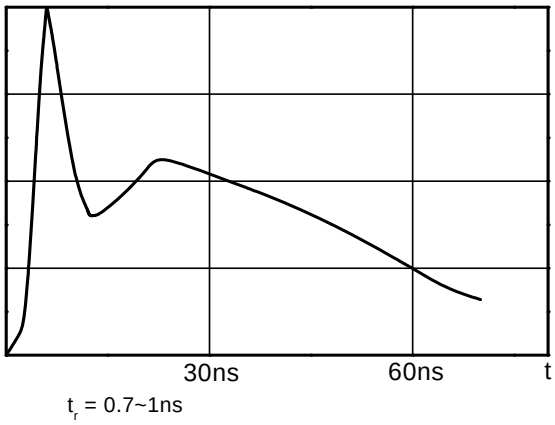
v

8/20 Ìs waveform per IEC61000 ¼4 5



Clamping voltage vs. Peak pulse current

Contact discharge current waveform per IEC61000 ¼4 2



Capacitance vs. Reverse voltage

Non repetitive peak pulse power vs. Pulse time

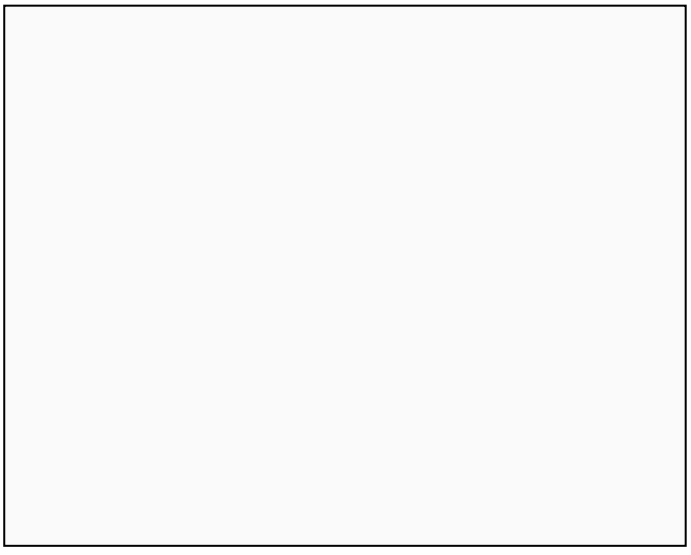
Power derating vs. Ambient temperature

ESD clamping
(+8kV contact discharge per IEC61000 ‐4 ‐2)

ESD clamping
(‐8kV contact discharge per IEC61000 ‐4 ‐2)

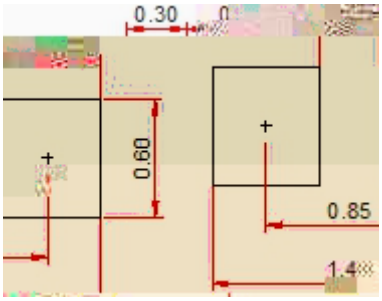
TLP Measurement

v



6\PERO PLQ PP 0D[PP

v



Notes:

This recommended land pattern is for reference purposes only.

The information presented in this document is for reference only. Yangzhou Yangjie Electronic Technology Co., Ltd. reserves the right to make changes without notice for the specification of the products displayed herein to improve reliability, function or design or otherwise.

The product listed herein is designed to be r h u s