N-Channel Enhancement Mode Field Effect Transistor

Product Summary

- V_{DS} 60V
- I_D (Silicon limited) 150A
- $R_{DS(ON)}$(at V_{GS}=10V) 3.5 mohm
- $R_{DS(ON)}$(at V_{GS}=4.5V) 5.0 mohm
- 100% EAS Tested
- 100% V_{DS} Tested
- ESD Protected up to 2.0KV(HBM)

General Description

- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for

■ Electrical Characteristics (T_j=25 unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	60			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60,V_{GS}=0V			1	μA
		V_{DS}=60,V_{GS}=0V, Tj=150			100	
Gate-Body Leakage Current	I_{GSS}	V_{GS}= 20V, V_{DS}=0V			10	μA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	1.0	1.7	2.5	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}= 10V, I_D=20A		2.7	3.5	mΩ
		V_{GS}= 4.5V, I_D=20A		3.5	4.8	mΩ
Diode Forward Voltage	V_{SD}	I_S=20A,V_{GS}=0V		0.8	1.3	V
Maximum Body-Diode Continuous Current	I_S					

Typical Performance Characteristics

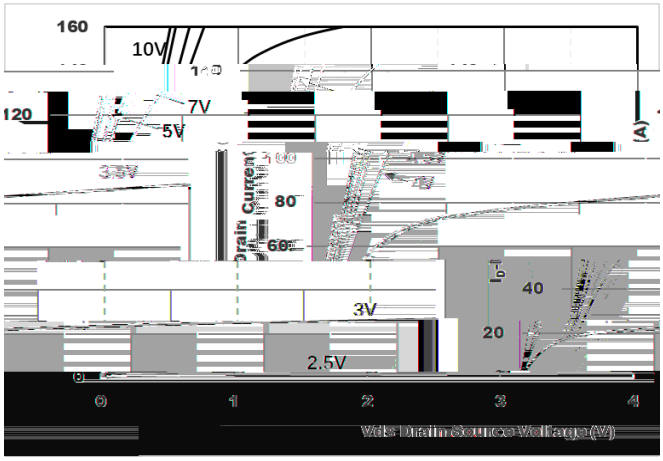

Figure1. Output Characteristics

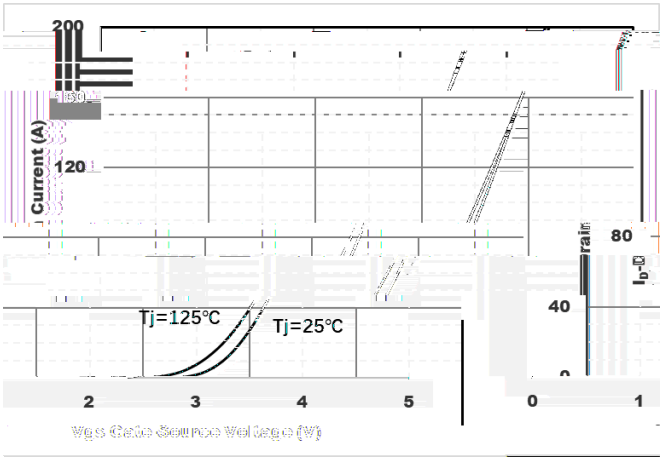

Figure2. Transfer Characteristics

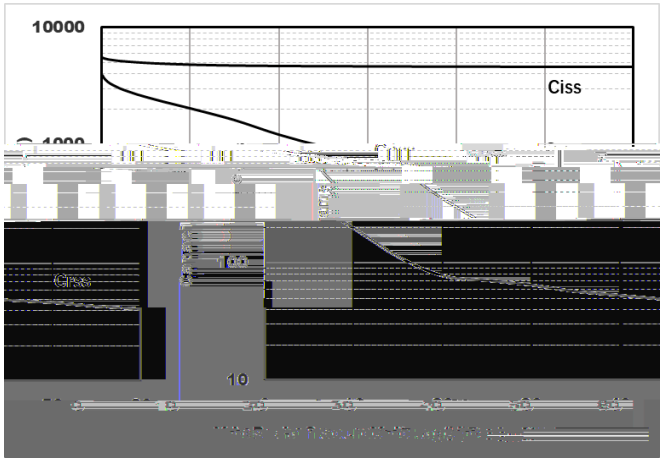

Figure3. Capacitance Characteristics

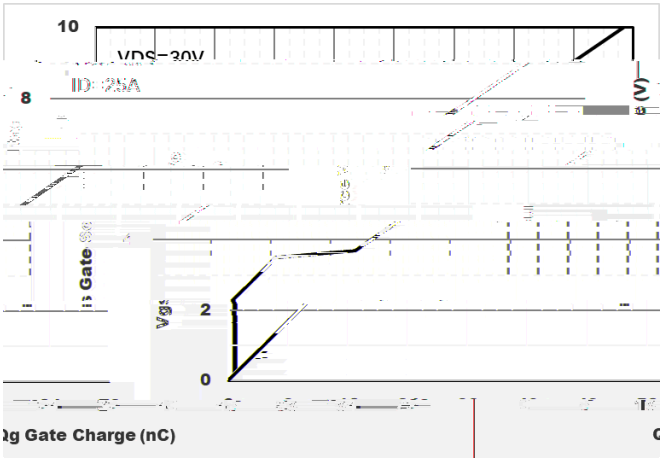

Figure4. Gate Charge

Figure5. On-Resistance vs. Drain Current and Gate Voltage

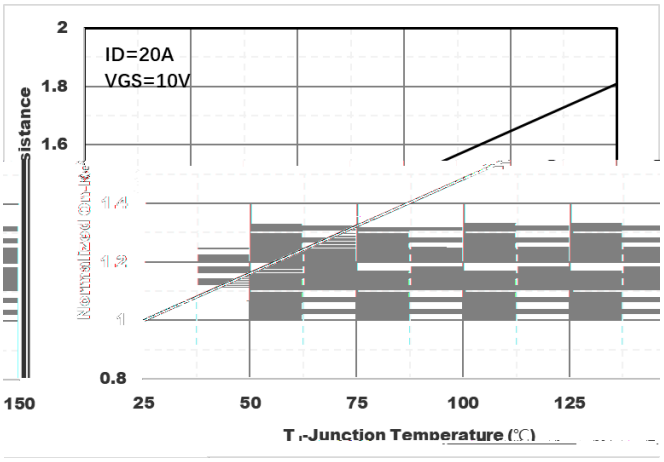

Figure6. Normalized On-Resistance

Figure13. Normalized Maximum Transient thermal impedance

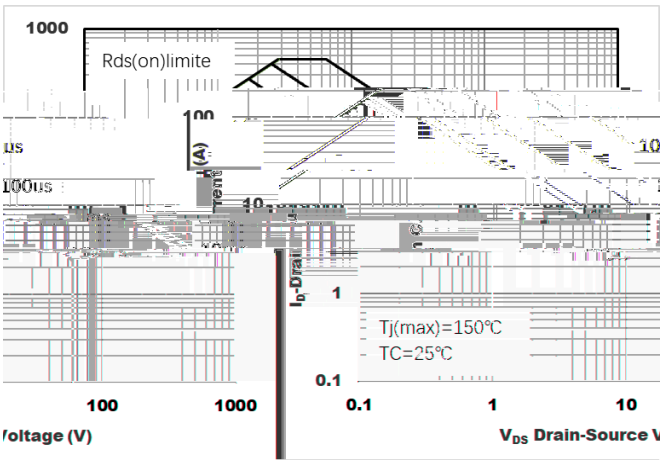

Figure14. Safe Operation Area

■ TO-263-HY Package information

SYM.	MIN.	
A2		
b2		0.050
c		
c2		
D2		
E		
E1		