N-Channel Enhancement Mode Field Effect Transistor

Product Summary

- V_{DS} 150V
- I_D 15A
- $R_{DS(ON)}$(at V_{GS}=10V) 70mΩ
- $R_{DS(ON)}$(at V_{GS}=6V) 80mΩ
- 100% EAS Tested
- 100% V_{DS} Tested

General Description

- Split gate trench MOSFET technology
- Low $R_{DS(on)}$ & FOM
- Excellent stability and uniformity
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Power management
- Portable equipment

■ Absolute Maximum Ratings (T_A=25 unless otherwise noted)

Parameter		Symbol	Limit	Units
Drain-source Voltage		V_{DS}	150	V
Gate-source Voltage		V_{GS}	±20	V
Drain Current	T_A=25	I_D	4	A
	T_A=100		2.5	
	T_C=25		15	
	T_C =100		9.5	
Pulsed Drain Current [A]		I_{DM}	40	A
Avalanche energy [B]		EAS	4.4	mJ
Total Power Dissipation [C]	T_A=25	P_D	2.5	W
	T_A=100		1	
	T_C=25		41	
	T_C =100		16	
Junction and Storage Temperature Range		T_J ,T_{STG}	-55 +150	

■ Electrical Characteristics (T_J=25 unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	150	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=150V, V_{GS}=0V	-	-	1	μA
		V_{DS}=150V, V_{GS}=0V, Tj=150	-	-	100	
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	2	3	4	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=15				

Typical Electrical and Thermal Characteristics Diagrams

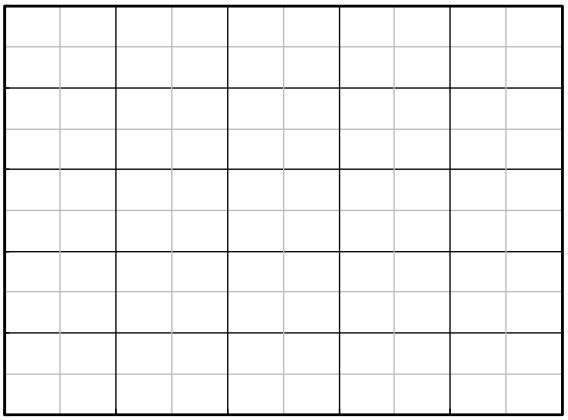


Figure 1. Output Characteristics

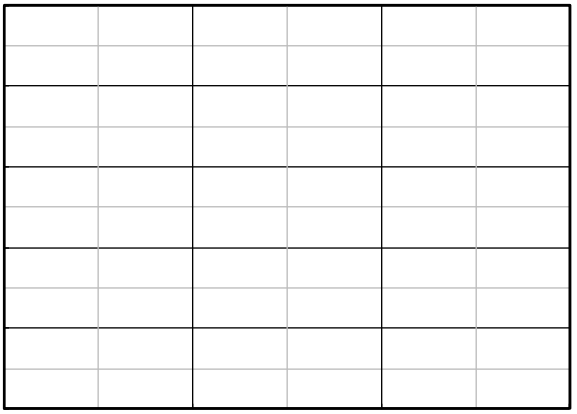


Figure 2. Transfer Characteristics

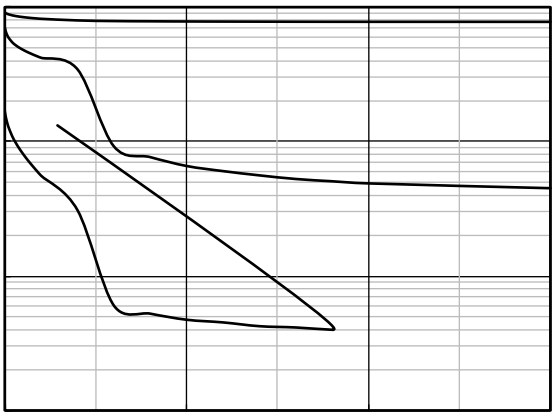


Figure 3. Capacitance Characteristics

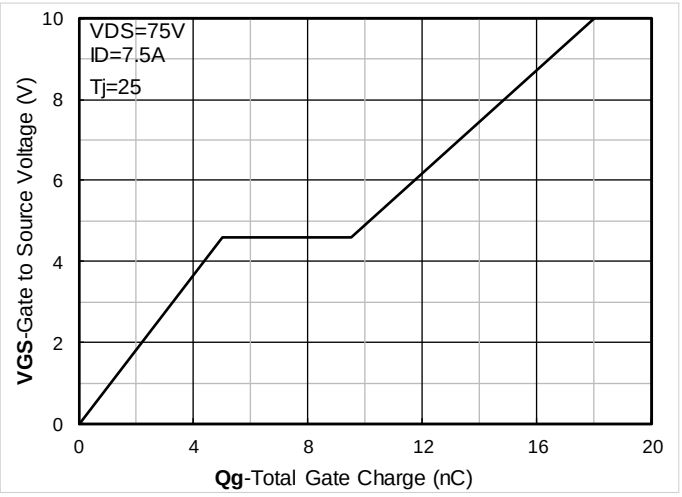


Figure 4. Gate Charge

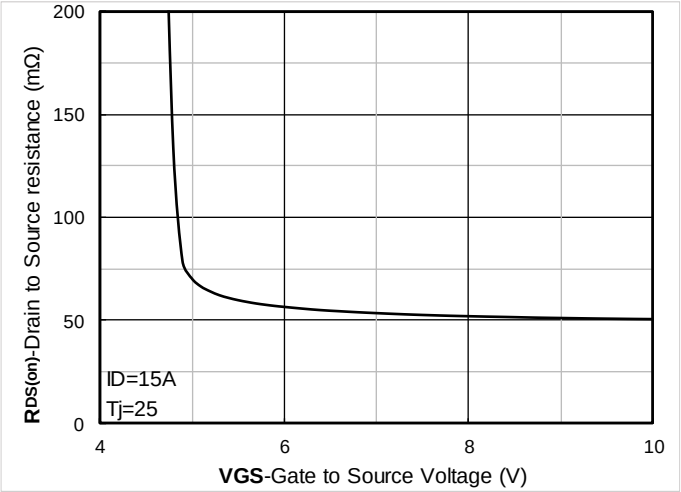


Figure 5. On-Resistance vs Gate to Source Voltage

Figure 6. Normalized On-Resistance

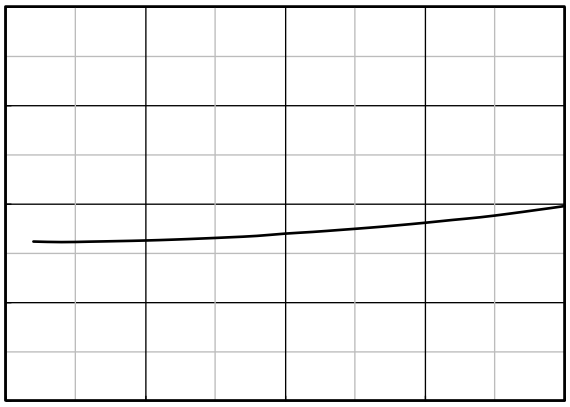


Figure 7. $R_{DS(on)}$ VS Drain Current

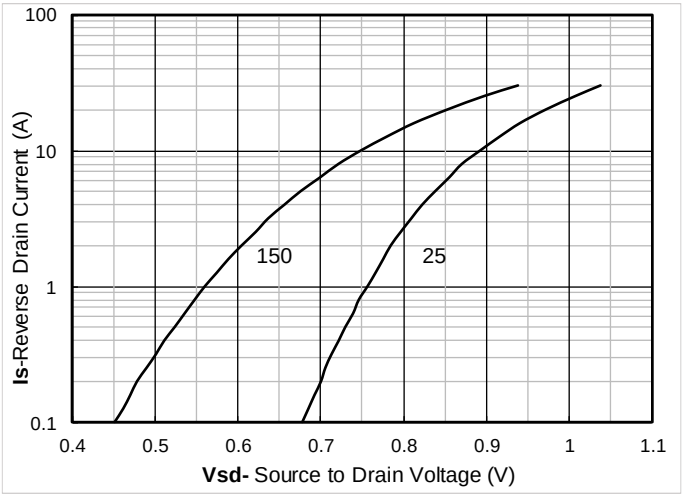


Figure 8. Forward characteristics of reverse diode

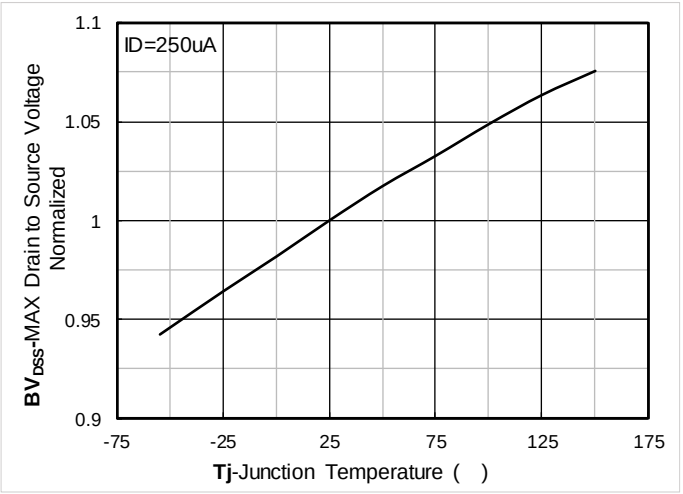


Figure 9. Normalized breakdown voltage

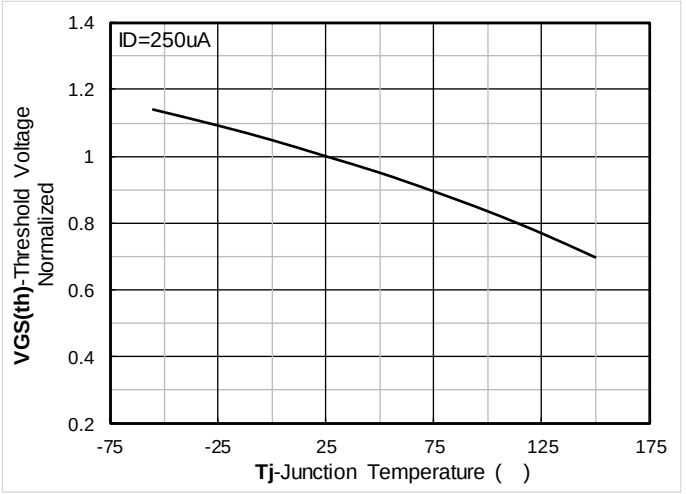


Figure 10. Normalized Threshold voltage

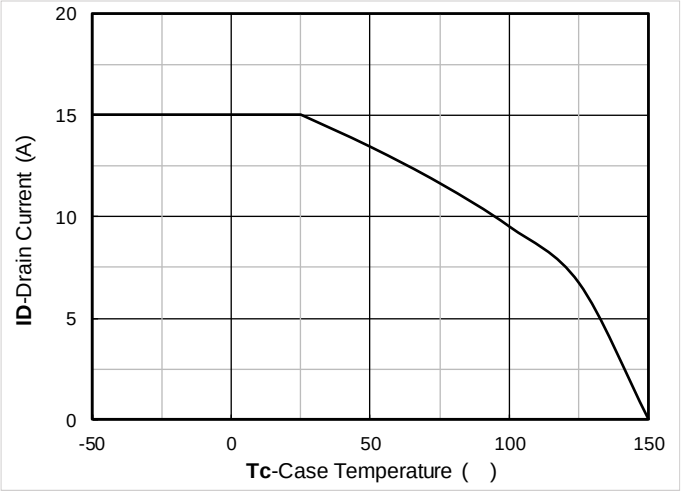


Figure 11. Current dissipation

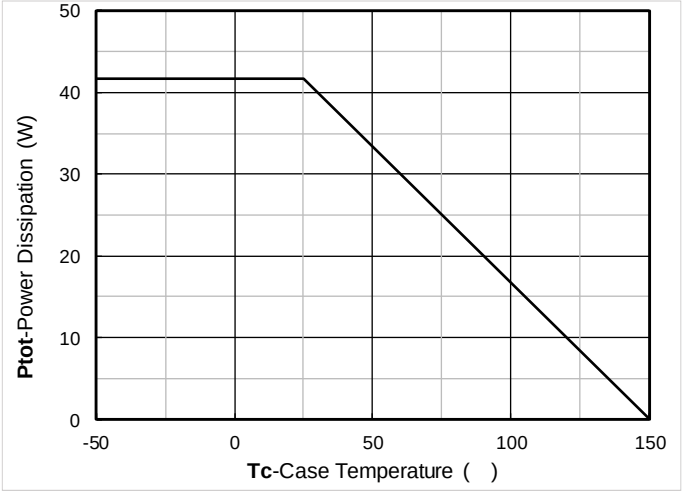


Figure 12. Power dissipation

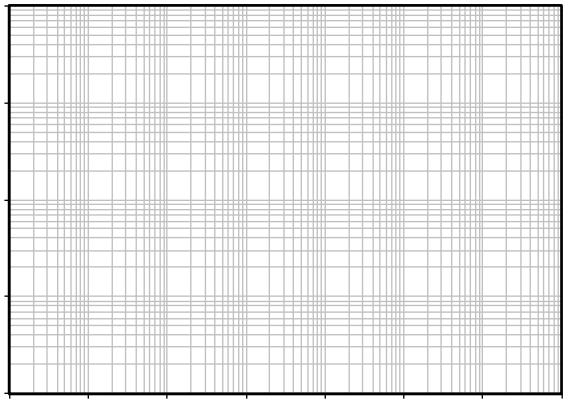


Figure 13. Maximum Transient Thermal Impedance

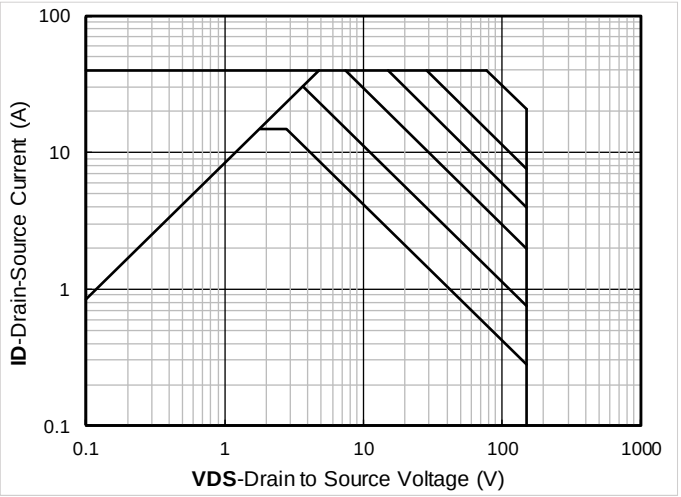


Figure 14. Safe Operation Area

■ Test Circuits & Waveforms

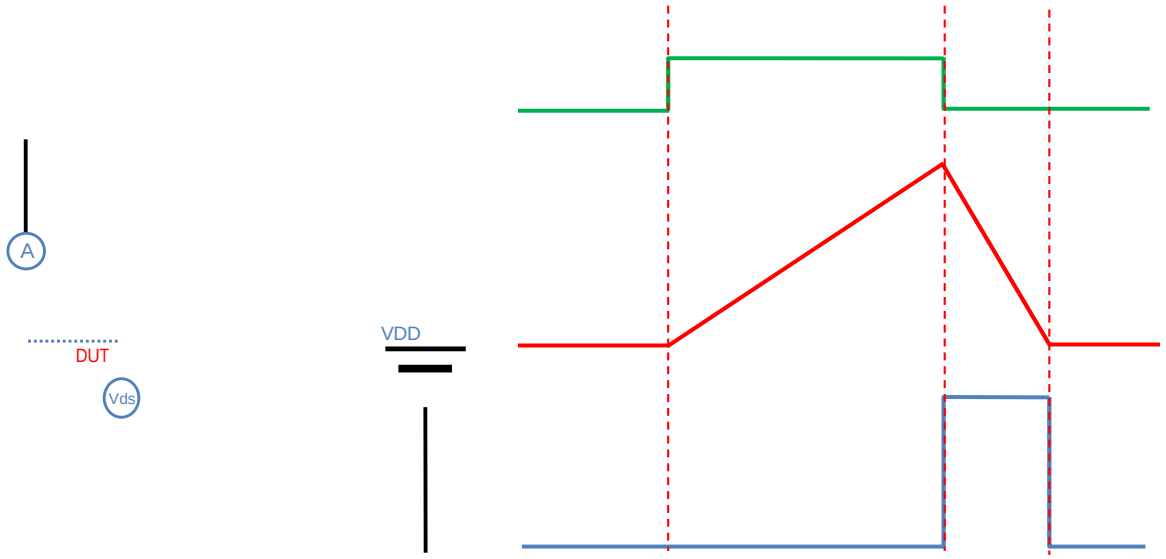
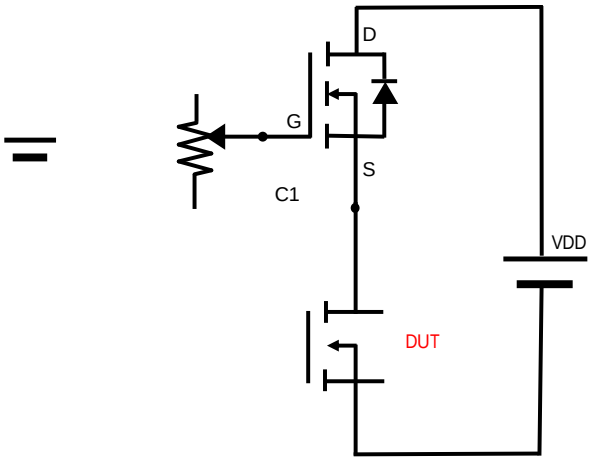
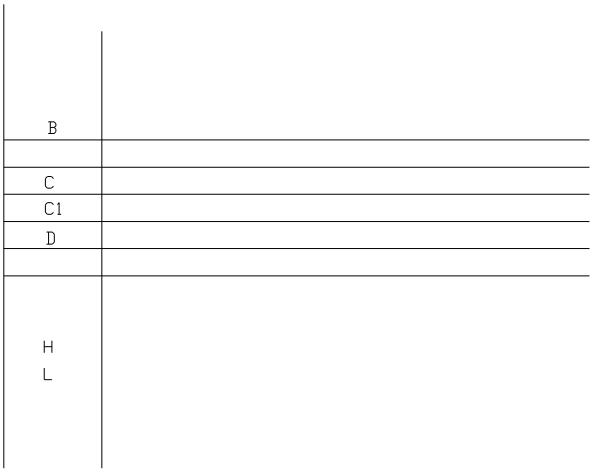


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform


D
G
S
C1
VDD
DUT

■ ITO-220AB-B Package information



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