



YJG2D5G06HQ

N-Channel Enhancement Mode Field Effect Transistor

Product Summary

V_{DS}	60V
I_D	160A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	2.5m
100% EAS Tested	
100% V_{DS} Tested	

General Description

Absolute Maximum Ratings ($T_A=25$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	60	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_A=25$	I_D	22	A
	$T_A=100$		16	
	$T_C=25$		160	
	$T_C=100$		114	
Pulsed Drain Current ^A		I_{DM}	500	A
Avalanche energy ^B		EAS	264	mJ
Total Power Dissipation ^C	$T_A=25$	P_D	2.5	W
	T_T			



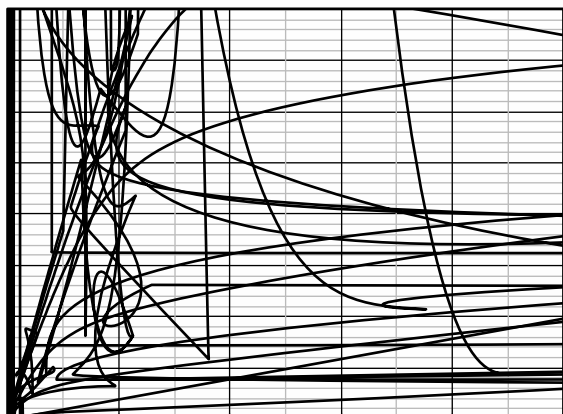
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Electrical Characteristics ($T_J=25$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						

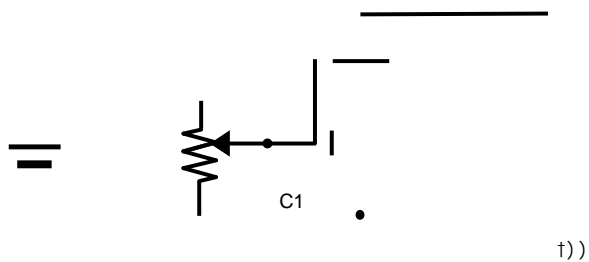


Typical Electrical and Thermal Characteristics Diagrams



4A&@Q-Uq)6•2'X`4



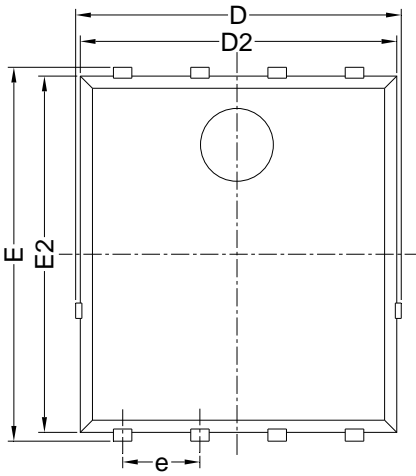


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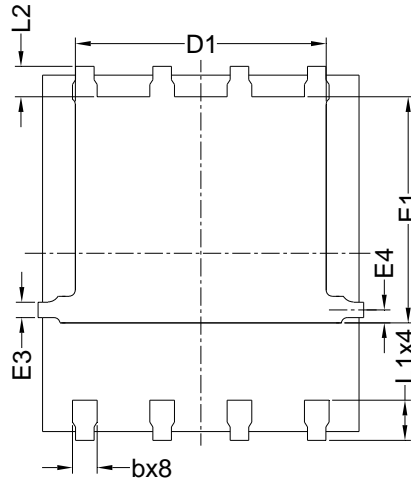


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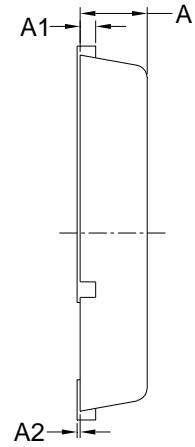
PDFN5060-8L-1.1MM Package information



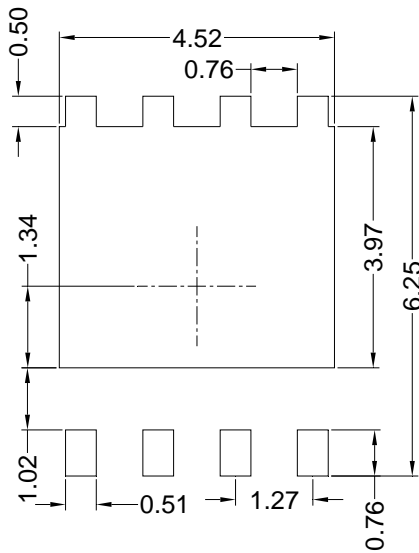
Top View



Bottom View



Side View



Suggested Solder Pad Layout
Top View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1	0.254 BSC		
A2			0.10
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
E3	0.254 REF		
E4	0.21 REF		
L1	0.56	0.66	0.76
L2	0.50 BSC		
b	0.31	0.41	0.51
e	1.27 BSC		

Note:

1. Controlling dimension: in millimeters.
2. General tolerance: ± 0.10 mm.
3. The pad layout is for reference purposes only.

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