N-Channel and N-Channel Complementary MOSFET

Product Summary

- V_{DS} 40V
- I_D 30A
- $R_{DS(ON)}$(at V_{GS}=10V) 13mΩ
- $R_{DS(ON)}$(at V_{GS}=4.5V) 20mΩ
- 100% EAS Tested
- 100% V_{DS} Tested

General Description

- Trench Power MV MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Power switching application
- Uninterruptible power supply

■ **Electrical Characteristics** (T_J=25 unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	40	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=40V, V_{GS}=0V	-	-	1	μA

Typical Electrical and Thermal Characteristics Diagrams

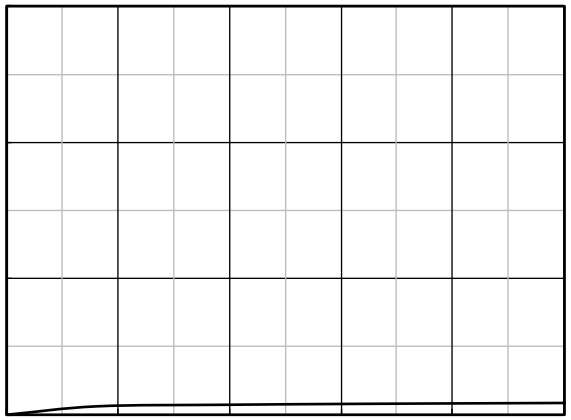


Figure 1. Output Characteristics

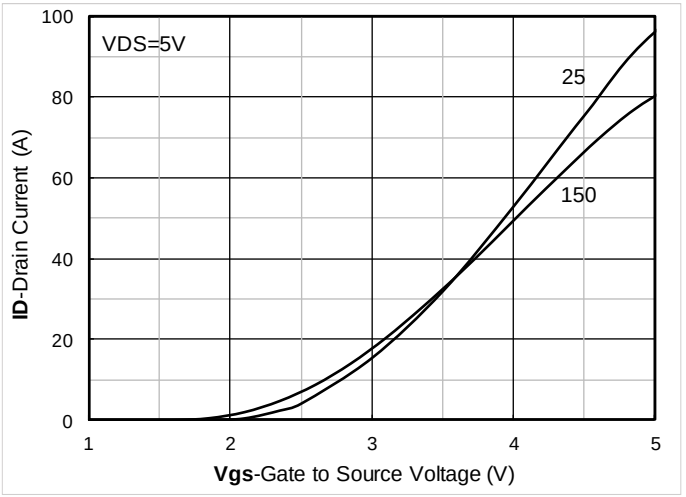


Figure 2. Transfer Characteristics

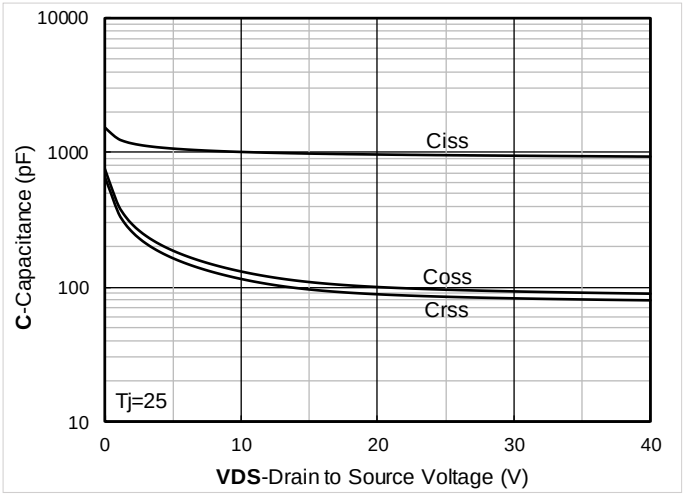


Figure 3. Capacitance Characteristics

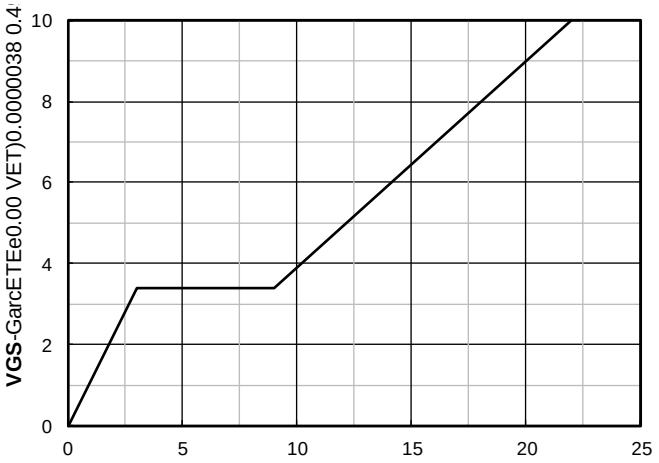
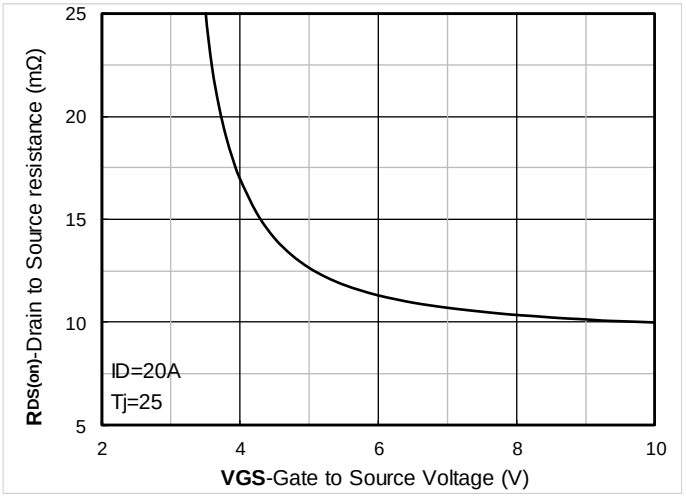


Figure 4. Gate Charge



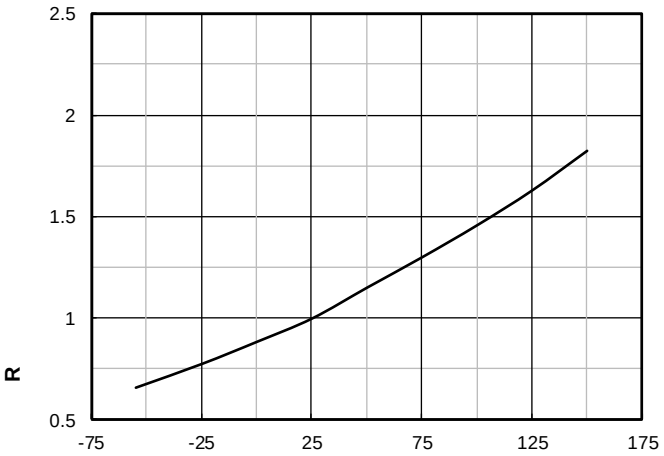


Figure 5. On-Resistance vs Gate to Source Volta-oi8882 slta-oi8882 slta-oi8882 slta-oi8882 slta-oi8882 slta-o882

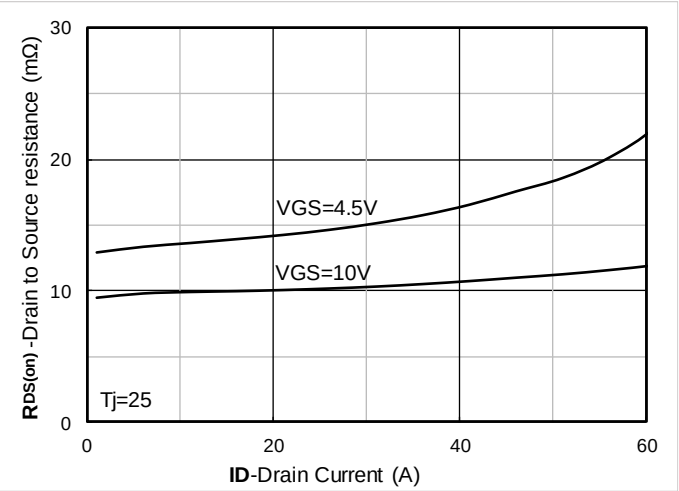

30
20
10
0
RDS(on) -Drain to Source resistance (mΩ)
VGS=4.5V
VGS=10V
Tj=25
0
20
40
60
ID-Drain Current (A)

Figure 7.

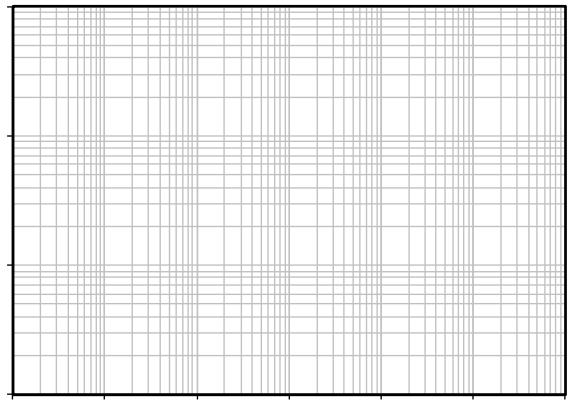


Figure 13. Maximum Transient Thermal Impedance

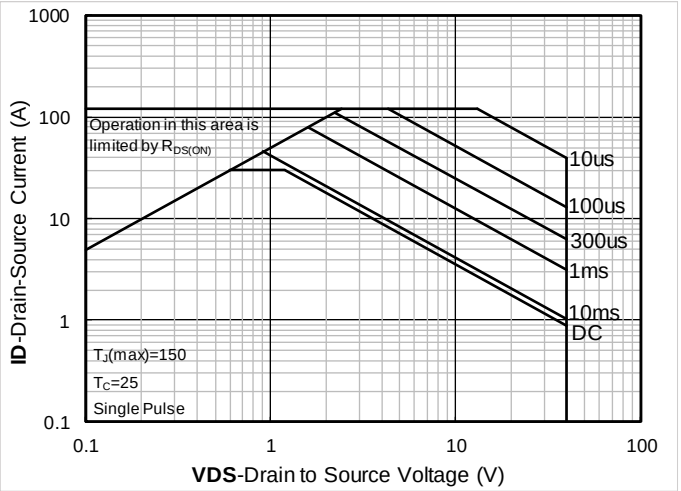


Figure 14. Safe Operation Area

■ Test Circuits & Waveforms

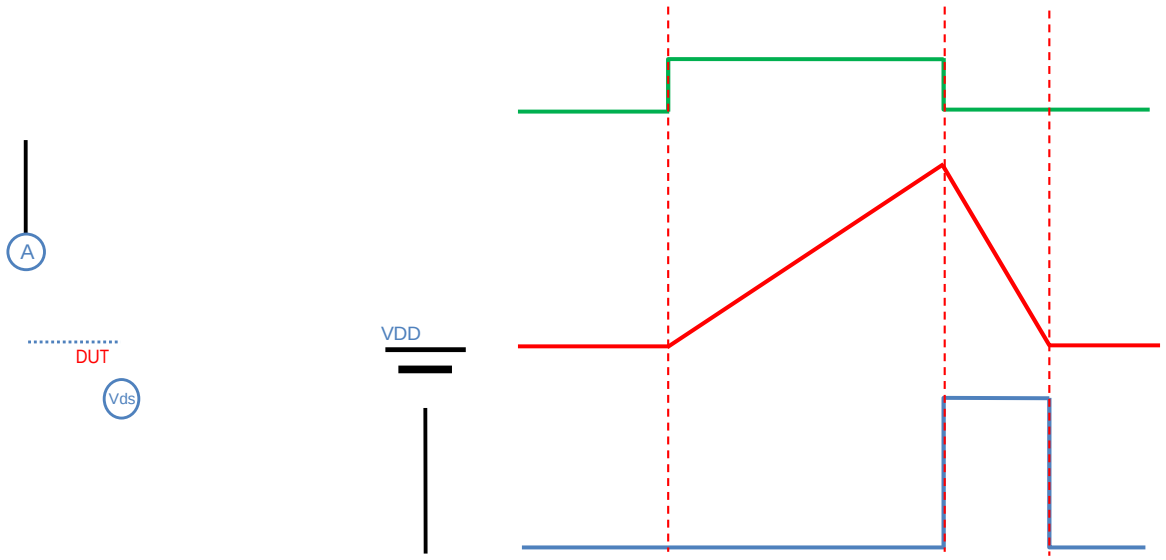


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

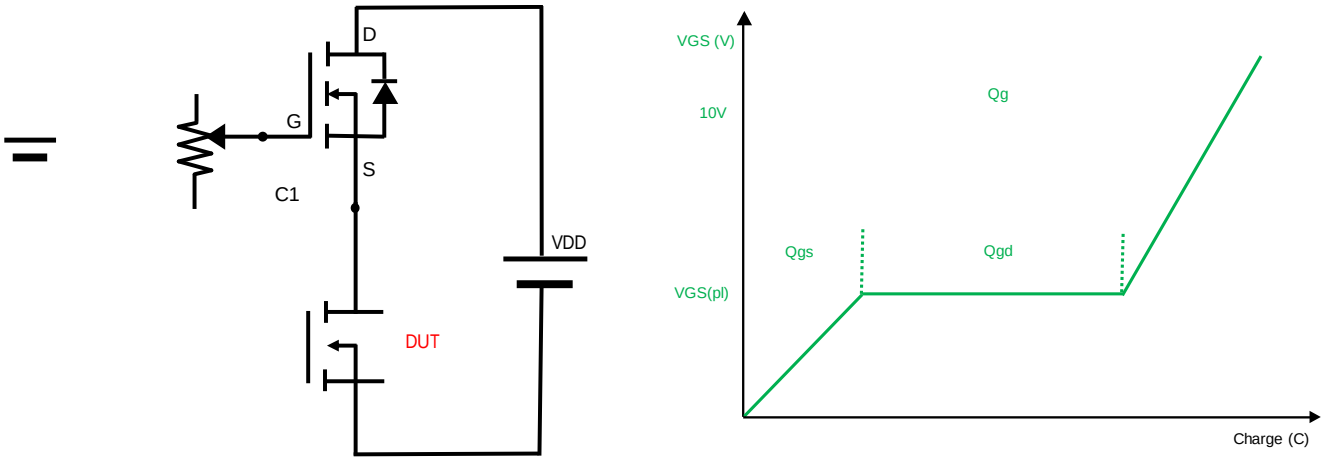
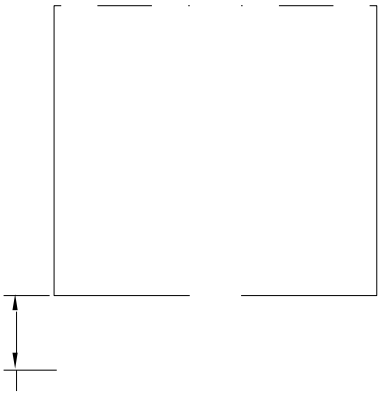


Figure B. Gate Charge Test Circuit & Waveform

■ PDFN5060-8L-E-1.1MM Package information



Suggested Solder Pad Layout
Top View

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.10mm.
3.The pad layout is for reference purposes only.