



# YJQ20N04AQ

## N-Channel Enhancement Mode Field Effect Transistor

### Product Summary

$V_{DS}$	40V
$I_D$	20A
$R_{DS(ON)}$ ( at $V_{GS}=10V$ )	15.0m
$R_{DS(ON)}$ ( at $V_{GS}=4.5V$ )	20.0m
100% EAS Tested	

### General Description

Excellent package for heat dissipation  
 High density cell design for low  $R_{DS(ON)}$   
 Part no. with suffix "Q" means AEC-Q101 qualified

### Applications

Power switching application  
 Uninterruptible power supply  
 DC-DC converter

### Ordering Information (Example)

PREFERRED P/N	PACKING CODE	M
YJQ20N04AQ	F1	Q

### Absolute Maximum Ratings

Parameter		Symbol	Limit	Unit
Drain-source Voltage		$V_{DS}$	40	V
Gate-source Voltage		$V_{GS}$	± 20	V
Drain Current	$T_C=25$	$I_D$	20	A
	$T_C=100$		17	
Pulsed Drain Current <sup>A</sup>		$I_{DM}$	80	A
Avalanche energy <sup>B</sup>		EAS		
Total Power Dissipation <sup>C</sup>	$T_A=25$	$P_D$		
	$T_C=25$			
Thermal Resistance Junction-to-Case	Steady-State	$R_{JC}$	5.9	/W



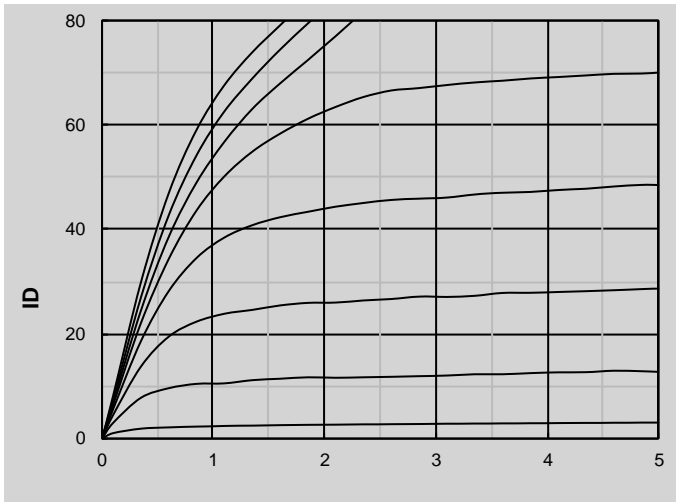
## YJQ20N04AQ

### Electrical Characteristics ( $T_J=25$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
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Typical Electrical and Thermal Characteristics Diagrams





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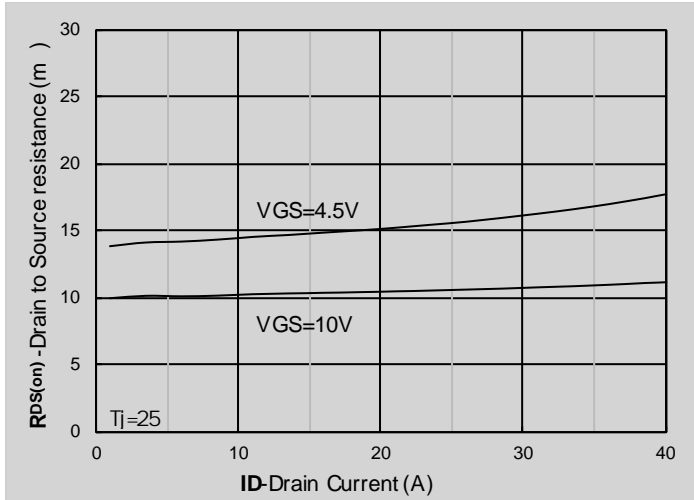


Figure 7.  $R_{DS(on)}$  VS Drain Current

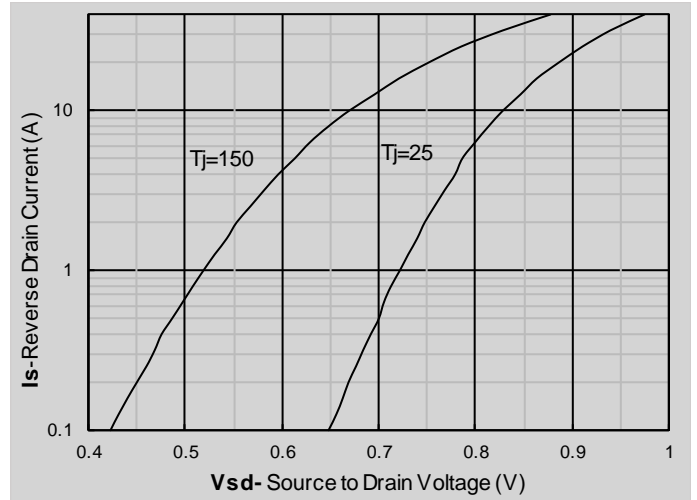
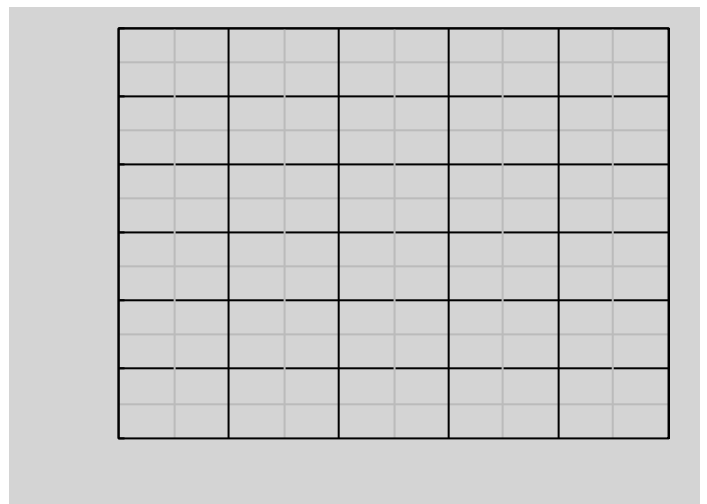
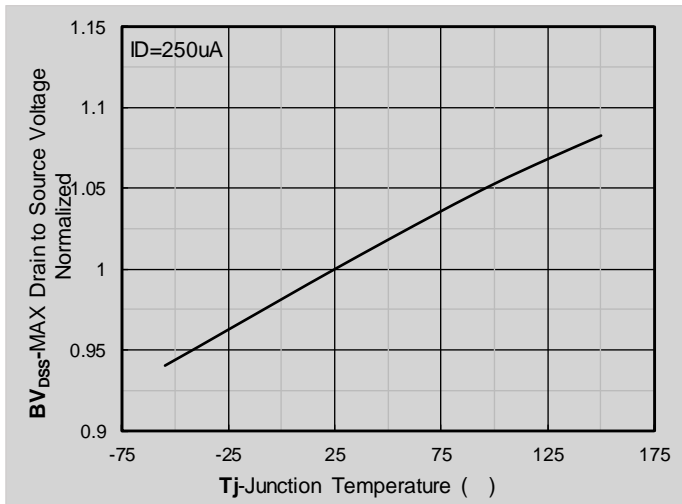


Figure 8. Forward characteristics of reverse diode



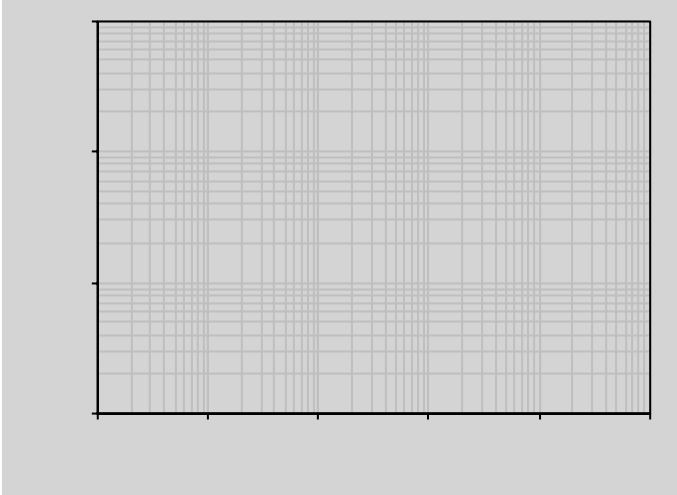


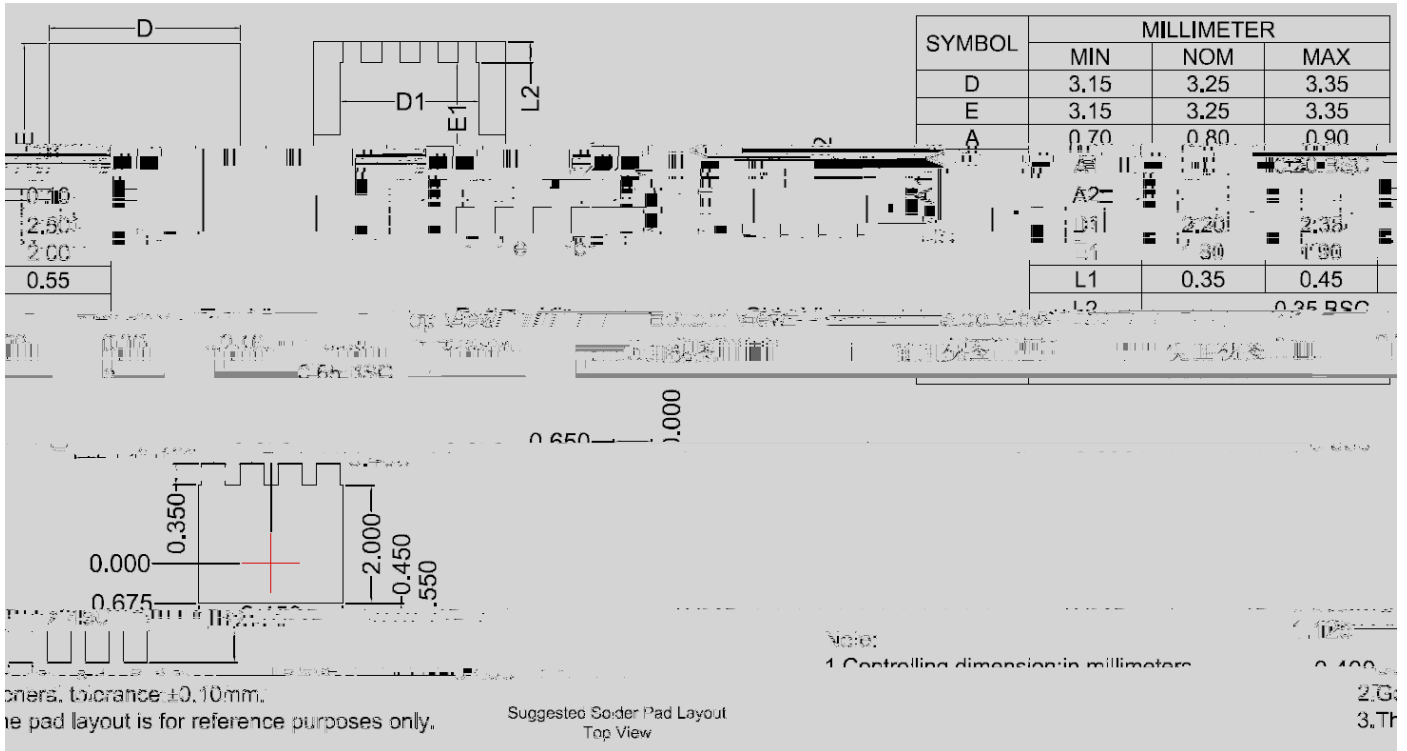
Figure 13. Maximum Transient Thermal Impedance

Figure 14. Safe Operation Area



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## DFN3333-8L Package information





**Disclaimer**

The information presented in this document is for reference onl

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