



N-Channel Enhancement Mode Field Effect Transistor

Product Summary

V_{DS}	40V
I_D	75A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	4.8m
100% EAS Tested	
100% V_{DS} Tested	

General Description

Excellent package for heat dissipation
High density cell design for low $R_{DS(ON)}$



YJQ4D8G04H

Electrical Characteristics ($T_J=25$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D$	40	-	-	V
		$V_{GS}=0V, I_D=1mA$	40	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=40V, V_{GS}=0V$	-	-	1	
		$V_{DS}=40V, V_{GS}=0V, T_J=125$	-	-	100	

Gate-Body Leakage Current



Typical Electrical and Thermal Characteristics Diagrams

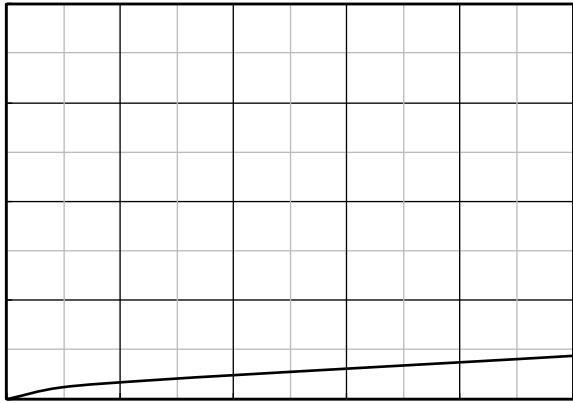


Figure 1. Output Characteristics

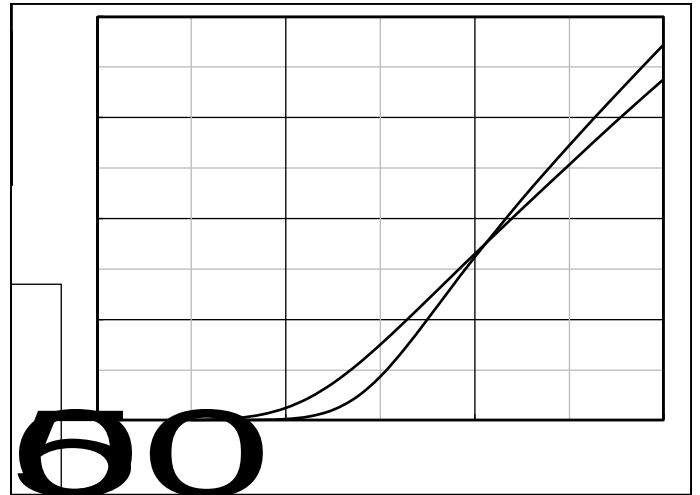


Figure 2. Transfer Characteristics

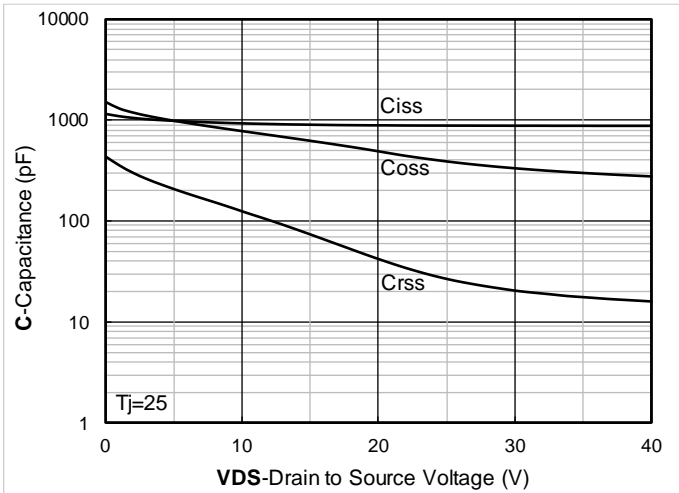


Figure 3. Capacitance Characteristics

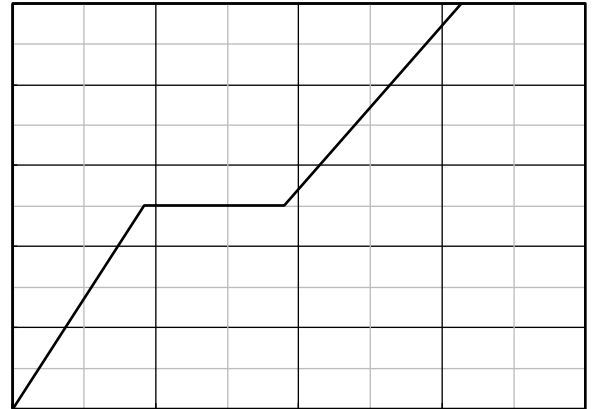


Figure 4. Gate Charge

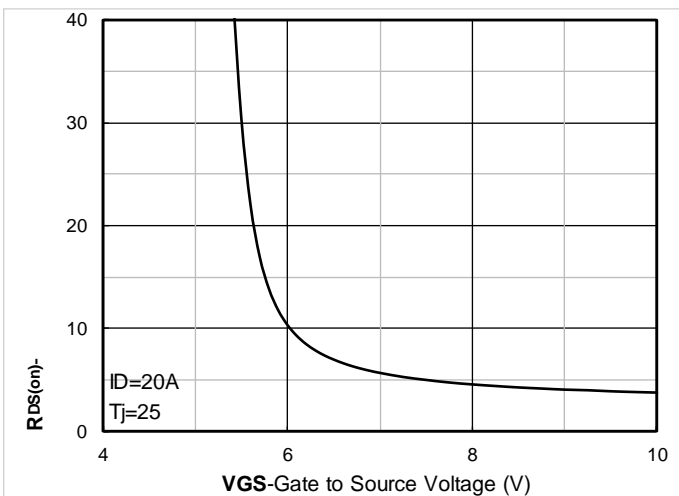


Figure 5. On-Resistance vs Gate to Source Voltage

Figure 6. Normalized On-Resistance



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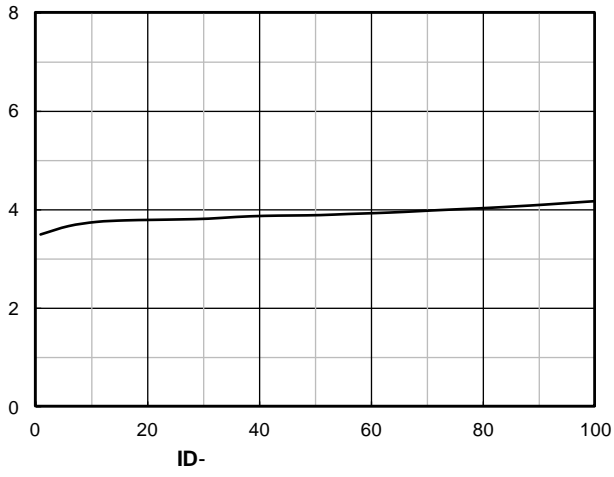
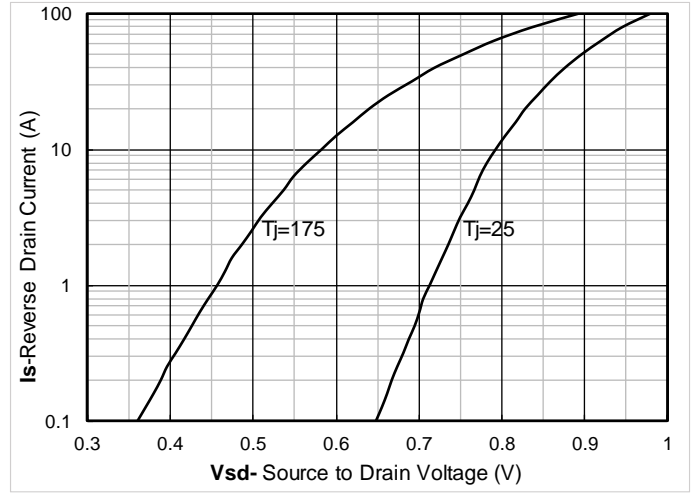


Figure 7. $R_{DS(on)}$



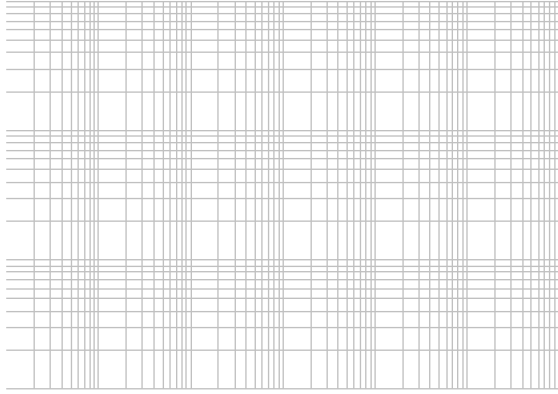


Figure 13. Maximum Transient Thermal Impedance

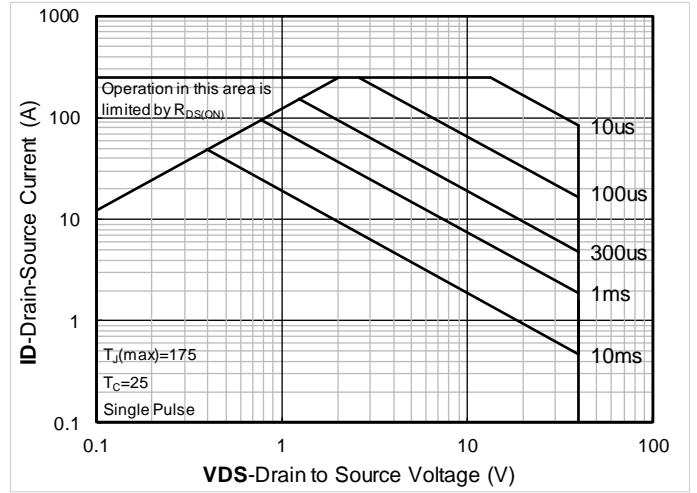


Figure 14. Safe Operation Area

Test Circuits & Waveforms

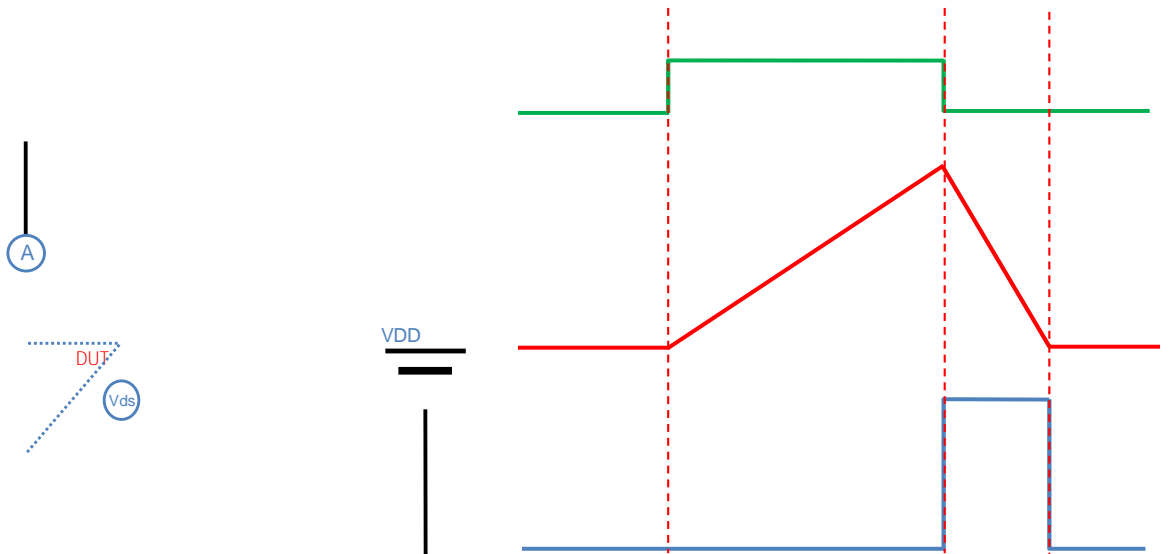


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

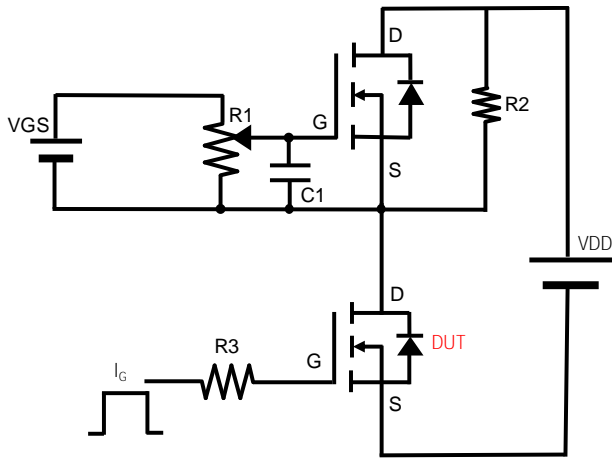


Figure B. Gate Charge Test Circuit & Waveform

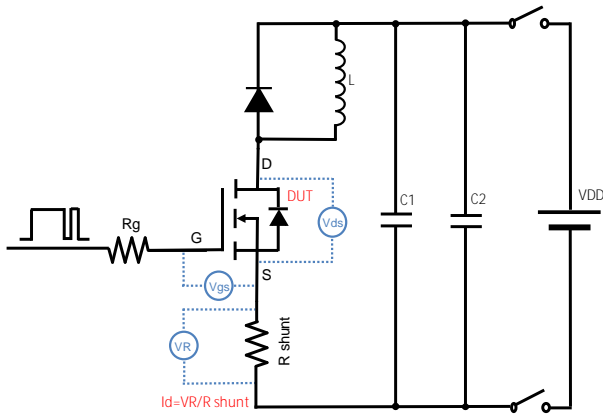


Figure C. Resistive Switching Test Circuit & Waveform

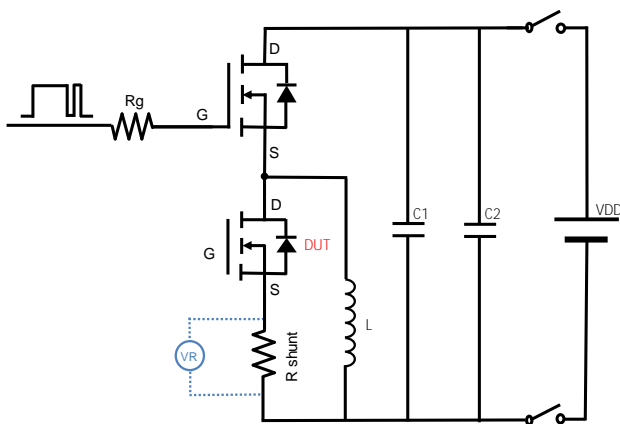
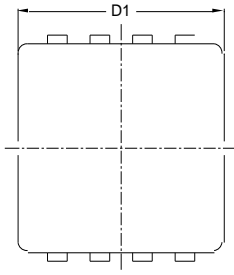


Figure D. Diode Recovery Test Circuit & Waveform

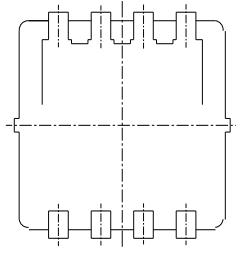


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PDFN3333-8L-B-0.75MM Package information



TOP VIEW



BOTTOM VIEW

SIDE VIEW

NOTE:

- 1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
- 2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
- 3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

UNIT mm

SUGGESTED SOLDER PAD LAYOUT



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